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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 10/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/900,945	SAITO, TOSHITADA	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6/8/2004.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 08 June 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the applicant's amendment dated 6/8/2004.

Claims 1-12 are pending.

Response to Amendment

1. The examiner acknowledges receipt of new drawing Figure 6 dated 6/8/2004 and approves said drawing.

2. The examiner acknowledges receipt of amendments to the specification dated 6/8/2004 and approves said amendments.

3. The examiner acknowledges the amendments to Claims 1 and 5.

4. Applicant's arguments, see amendment filed 6/8/2004, with respect to the rejections of claims 1, 2 and 10 under 35 USC § 102(e) have been fully considered and are persuasive. Therefore, the rejections have been withdrawn, as well as rejections of the dependent Claims 3-9 and 11-12. However, upon further consideration, a new ground of rejection is made in view of Iwata et al., U.S. Patent No. 6687857 (see below).

Claim Rejections - 35 USC § 103

1. Claims 1-4, and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motoki Higashida, U.S. Patent No. 6523136, in view of Iwata et al., U.S. Patent No. 6687857.

As per Claim 1:

Higashida teaches an LSI circuit (column 1 line 20) comprising a storage circuit, peripheral circuits (see FIG. 1), a processor circuit (column 1 lines 5-17) with a program counter, ALU, and register (column 1 lines 18-21 and FIG. 2). There is a selection means for each of the above (column 1 lines 22-37, column 7 lines 15-30, and Fig.'s 2 & 3), as well as selector control by way of a signal via an external terminal (see FIG. 1 9). But Higashida fails to teach the LSI as being formed on one chip, and a selection and controller, for outputting a result signal on the basis of a select signal from outside. But the analogous art of Iwata et al. does teach these features in column 3 lines 35-67, and columns 4-6. The one chip system (column 7 line 54) utilizes a JTAG select signal (TMS) from outside to program which of the units is selected (via Monitor Valid Control Unit 114 through Monitor Data Unit 85) to output results to the outside. And column 3 lines 37-46 cites the advantage of a processor which can self-debug using outside debugging instructions. One with ordinary skill in the art at the time of the invention, motivated as suggested, would incorporate the chip as described by Iwata et al. into the system taught by Higashida, in order to provide more flexibility to the debug of the chip.

As per Claim 2:

Claim 2, being dependent on Claim 1 above, is further taught by Iwata et al., the system to comprise a debug circuit within the MPU that further controls the selector control circuit, and being under control of the processor, as well as the external terminal (FIG.2 Debugging Module 54). And in view of the motivation previously stated, the claim is rejected.

As per Claim 3:

Claim 3, dependent on Claim 1 above, further limits the system to have three selection units, the 1st to select one of the program counter, register, storage, or processor, the 2nd to select one of the peripheral circuits, and the 3rd to select one of the 1st or second. Higashida teaches all of these selectors, the 1st in FIG. 2 and column 7 lines 15-30, the 2nd in FIG. 3 under control of TP1 and column 7 lines 55-62, and the 3rd in FIG. 3 under control of TP2 and column 7 lines 62-67. Instead of the storage being selected in the 1st selector as claimed by the applicant, Higashida instead selects the storage units by way of selector 2, and so is not precisely the same as the Claim 3. In would have been obvious to one with ordinary skill in the art at the time of the invention, motivated to use the same bus for storage as for peripherals, to select the Higashida configuration. The examiner does not see any electrical difference in the drawings between the applicant's or the Hgashida configuration, and believes that the applicant's configuration may be the same. Being electrically the same, the Claim 3 is rejected.

As per Claim 4:

Claim 4, dependent on Claim 3 above, further limits the system to a debug backup circuit that is controlled by the processor, and controls selection of the 1st through 3rd selectors as well as the outside signal. Higashida fully teaches this in FIG. 8, by adding the "Register Circuit" 8c in an embodiment of that patent, which derives control from the processor bus (see column 10, lines 54-67 and column 11, lines 1-54), and selects either under control of the processor or external signal. And in view of the motivation previously stated, the claim is rejected.

As per Claim 10:

Claim 10, dependent on Claim 1 above, is further taught by Iwata et al. wherein the system has I/O terminal(s) for sending signals to and from a peripheral device. Iwata et al. also explicitly teaches this in FIG.1 Bus Control 58 and column 7 lines 51-67. And in view of the motivation previously stated, the claim is rejected.

As per Claim 11:

Claim 11, dependent on Claim 10 above, further limits the I/O terminal(s) to being used for inputting/outputting control and monitor signals. Higashida teaches inputting controls (column 11 lines 1-54) for multiplex controls, outputting monitor signals is not specifically taught. However, the system of Higashida has the same structure as the applicant's, and therefore, under control of the processor, as in column 7 lines 15-67, the same bus which multiplexes monitor data to the monitor output can under the processor control output the data via the I/O bus. One with ordinary skill in the art at the time of the invention, motivated to providing test data without using any more I/O pins as suggested by Higashida in column 4 lines 3-30, would have used only the available I/O pins for test data, or both I/O pins and monitor pins, therefore the Claim 11 is rejected.

As per Claim 12:

Claim 12, dependent on Claim 1, limits the system to one monitor input control signal, and one monitor output terminal during debug. Higashida teaches the input control signal (FIG. 1 9), but uses an 8-bit monitor output bus (FIG. 1 12). However, one with ordinary skill in the art at the time of the invention, motivated to providing test data without using any more I/O pins as suggested by Higashida in column 4 lines 3-30,

would have used only the available I/O pins for test data, or both I/O pins and one monitor pin, therefore the Claim 12 is rejected.

2. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motoki Higashida, U.S. Patent No. 6523136, in view of Iwata et al., U.S. Patent No. 6687857 as applied to claims 1 and 3 above, and further in view of Tashiro et al., U.S. Patent No. 5566303.

As per Claims 5 and 6:

Claims 5 and 6 further limit Higashida to multiple processor units on the LSI circuit according to Claim 3, including multiple selection units, control signals, debug units, control circuits, as well as the external monitor control signal. Higashida in the dependent claims above teaches all of this, but does not teach multiple processors. Tashiro et al. does teach multiple processors (see FIG. 11 and 12) in column 1 lines 9-16. One with ordinary skill in the art at the time of the invention, motivated to providing test capabilities to all processors resident on a chip, as suggested by Tashiro et al. (see Abstract), would combine the processors of Tashiro et al. with the system configuration of Higashida, therefore the Claims 5 and 6 are rejected.

As per Claim 7:

Claim 7, dependent on Claim 5, limits the system to a serial to parallel converter for outputting to the outside. Higashida does output an 8-bit signal (see FIG.1 12), and therefore by virtue of the output bus size, does not require a serial/parallel conversion. If one were required, then as suggested for larger bus widths in column 8 lines 18-29 of Higashida, one would utilize a serial/parallel converter; therefore the Claim 7 is rejected.

As per Claim 8:

Claim 8, dependent on Claim 5, limits the system to a parallel to serial converter for outputting to the outside. Higashida does output an 8-bit signal (see FIG.1 12), and would therefore require a parallel/serial conversion. One with ordinary skill in the art at the time of the invention, motivated to providing test data without using any more I/O pins as suggested by Higashida in column 4 lines 3-30, would have used only the available I/O pins for test data, or both I/O pins and one monitor pin, and would require a standard parallel/serial converter. Therefore the Claim 8 is rejected.

As per Claim 9:

Claim 9, dependent on Claim 5 above, further limits the system to use of a thinning-out circuit. Higashida, in column 11 lines 56-67, column 12 lines 1-67, and column 13 lines 1-32, describes the use of flip-flops in-line with monitor data, triggered by a clock. As suggested by column 15, lines 1-6, the examiner recognizes the arrangement of flip-flops to be also a thinning-out circuit, however Higashida does not specify it as such. One with ordinary skill in the art at the time of the invention, motivated to reducing bandwidth of output data would be inclined to change the clock speed of the Higashida invention in order to thin out the signal, therefore the Claim 9 is rejected.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

GUY J. LAMARRE
PRIMARY EXAMINER